REMARKS

Rejections

Rejections under 35 U.S.C. § 103(a)

Claims 2-4, 9, 11, 13, 16, 17, 23, and 25

Claims 2-4, 9, 11, 13, 16, 17, 23, and 25 stand rejected under 35 U.S.C. § 103(a) as being obvious over Priem et al. (EP 0525986) in view of Rao, (WO 97/06523). Applicant respectfully submits that the combination is improperly motivated and furthermore does not teach each and every element of the invention as claimed in claims 2-4, 9, 11, 13, 16, 17, 23, and 25.

Priem discloses a double buffered display system comprising a central processing unit (CPU) with two frame buffers, in which the first frame buffer is less expensive dynamic random access memory (DRAM) and the second frame buffer is more expensive video random access memory (VRAM). Both display systems use DRAM to replace VRAM in one of the frame buffers. However, Priem does not disclose either frame buffer as being part of the general main system memory.

Rao discloses a unified system and frame buffer memory system using a single memory controller where the frame buffer and system memory are collocated in a single integrated circuit or single bank of circuits. Rao contrasts the unified system with the prior art that used two memory controllers and where the frame buffer is physically separate from the system memory. Furthermore, Rao discloses that the unified memory system overcomes inefficiencies presented with separate memory devices.

The combination of Priem and Rao is improperly motivated because there is no motivation to combine Rao with Priem. The Examiner proposes replacing Priem's CPU with Rao's core logic, CPU, display controller and memory unit, such that Rao's core logic works with Priem's multiple buffer architecture. However, Rao discloses that using a memory controller (i.e. Rao's core logic) in a unified memory system is more efficient than using a memory controller with separate memory devices. Thus, Rao teaches away from using multiple memory devices. Because Priem uses separate memory devices (i.e.

multiple frame buffers), there is no motivation to combine Priem's separate memory devices with Rao's memory controller.

Nonetheless, assuming for the sake of argument that if the combination is properly motivated, the combination fails to teach or suggest each and every element as claimed. In independent claims 2, 11, 16, and 23, Applicant claims a sole memory controller that maps the frame preparation memory to the main memory and the refresh memory to memory separate from the main memory. While Priem discloses two frame buffers, Priem fails to teach or suggest a frame buffer mapped onto main memory. Furthermore, Priem does not teach or suggest a memory controller. In addition, as stated in a previous response, Rao fails to teach or suggest mapping with one memory controller as claimed because Rao discloses (i) a unified memory system with one memory controller that collocates system memory and frame buffer onto single bank of circuits or a single integrated circuit (Rao, p. 11, lines 26-29) and (ii) prior art that has physically separate system memory and frame buffers using two memory controllers.

Thus, the combination cannot be properly interpreted as disclosing claims 2, 11, 16, and 23 and claims 3, 4, 9, 13, 17, and 25 that depend on them. Therefore, the combination cannot render obvious Applicant's invention as claimed in claims 2-4, 9, 11, 13, 16, 17, 23, and 25, and Applicant respectfully requests the withdrawal of the rejection of the claims under 35 U.S.C. § 103(a) over the combination.

Claims 5-8, 12, 14, 18-21, 24, and 26

Claims 5-8, 12, 14, 18-21, 24, and 26 stand rejected under 35 U.S.C. § 103(a) as being obvious over Priem in view of Rao and Akeley, US Patent No. 6,075,543. Applicant respectfully submits that the combination does not teach each and every element of the invention as claimed in claims 5-8, 12, 14, 18-21, 24, and 26.

Akeley discloses managing multiple frame buffers by maintaining a queue of buffers. However, Akeley does not disclose how the buffers are mapped onto physical or graphics memories.

Claims 5-8, 12, 14, 18-21, 24, and 26 depend from independent claims 2, 11, 16, and 23. In independent claims 2, 11, 16, and 23, Applicant claims a sole memory controller that maps the frame preparation memory to the main memory and the refresh

memory to memory separate from the main memory. As per above, neither Priem nor Rao teach or suggest this claim limitation. Furthermore, because Akeley does not disclose whether the multiple buffers are mapped onto physical or graphics memory, Akeley cannot teach or suggest mapping frame preparation memory onto main memory and refresh memory to memory separate from main memory as claimed.

Thus, the combination cannot be properly interpreted as disclosing independent claims 2, 11, 16, and 23 and claims 5-8, 12, 14, 18-21, 24, and 26 that depend on them. Therefore, the combination cannot render obvious Applicant's invention as claimed in claims 5-8, 12, 14, 18-21, 24, and 26, and Applicant respectfully requests the withdrawal of the rejection of the claims under 35 U.S.C. § 103(a) over the combination.

SUMMARY

Claims 2-9, 11-14, 16-21 and 23-26 are currently pending. In view of the foregoing remarks, Applicant respectfully submits that the pending claims are in condition for allowance. Applicant respectfully requests reconsideration of the application and allowance of the pending claims.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact Eric Replogle at (408) 720-8300 x7514.

Deposit Account Authorization

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicant hereby requests such extension.

Respectfully submitted,

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